Cascaded Dual Model Predictive Control of an Active Front-End Rectifier

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***Abstract*—Model Predictive Control (MPC) is an advanced model-based control technique. It allows flexible control schemes with fast time responses. However, as most optimization-based control strategies, MPCs are usually computationally intensive and suffer from a lack of robustness towards parametric variations. The computational burden of these controllers is nowadays being relieved thanks to the progress of digital devices however, the robustness is still a major issue that prevents the use of MPC controllers in some applications. Systems presenting slow and fast dynamics at the same time are usually controlled by cascaded control loops. MPC techniques are restricted to the control of inner-loops while outer-loops use more robust control techniques. The aim of this paper is to provide MPC techniques for both the inner and outer loops of an active front-end rectifier. A first dual MPC cascaded control shows the drawbacks of usual MPC techniques for outer-loops. It is thereafter modified to achieve a robust cascaded dual-MPC that eliminates the variable resistive load parameter from the system dynamical model and formulates a new prediction model containing only known parameters and measurable quantities. Finally, a third method based on the previous one is also presented in order to reduce switching losses. Experimental results for the three methods are presented and compared with double precision off-line software simulation results to validate the feasibility of the proposed techniques.**

***Index Terms*—Predictive control, Active-Front-End rectifier, optimization techniques**

I. Introduction

MODEL Predictive Control (MPC) is an advanced optimization-based control strategy that was extensively used for the last three decades in chemical and petrochemical industries [1], [2]. Indeed, MPC techniques offer a series of advantages over other methods. They allow flexible, easy to tune control schemes with fast time responses. They can therefore be applied to a variety of linear or non-linear systems with constraints [3].

MPC techniques suffer however from two main drawbacks. As all optimization-based control techniques, MPC algorithms are computationally intensive. For this reason, MPC were firstly restricted to the control of slow dynamic systems. Throughout the last decade and thanks to the ceaseless progress of digital devices such as Field Programmable Gate Arrays (FPGAs) [4] and Digital Signal Processors (DSPs) [5], the application of MPC techniques to electrical systems became possible but stays challenging. Since then, many MPC techniques for the control of numerous electrical systems such as power electronics [6], [7] and adjustable speed drives [8]–[10] have been presented.

Moreover, MPC techniques are model-based control strategies. Therefore, the model is not used exclusively for tuning purposes but acts as the corner stone of the controller since it is used to predict the future behavior of the system. The control performances are then closely related to the quality of the plant model knowledge and consequently an accurate plant model implies better predictions. As all model-based control techniques, these controllers introduce a lack of robustness towards parameter variations and measurement noises. This prevents their use in some applications such as the control of systems presenting slow and fast dynamics at the same time like power rectifiers connected to the grid [6], [11], adjustable speed drives [8], [12], etc.

For this kind of applications, the chosen control structure is usually a cascaded control technique based on dual decoupled loops; an inner-loop to control variables with fast dynamics and an outer slower loop that deals with variables presenting slow dynamics. MPC techniques are usually restricted to the control of the inner-loops while outer-loops use robust control techniques such as PI controllers [10], [11], [13] to counteract the effect of the bias introduced in the inner-loop resulting from the non-accuracy of the prediction model.

In [14], the grid currents and the DC-link voltage of an active front-end rectifier supplying a resistive load are controlled using MPC techniques. This paper presents a robust MPC voltage outer-loop that deals with variations in the DC-link load resistance but does not take into consideration the variation of other parameters. The measurement noise which is a major issue in robustifying an MPC algorithm was not treated. In [15], the control of a DC-DC step-down voltage converter is developed. The authors propose the use of a static Kalman filter in order to robustify the MPC control algorithm. [6] presents a survey on different MPCs for power electronics applications. The paper develops cascaded control applied to active front-end rectifier, matrix converter, etc. Many MPC techniques for the control of the current inner-loop are shown while the voltage outer-loop is systematically controlled using a classic PI controller. In [12] and [13], MPC techniques are applied to the control of the current inner-loop in drive

Manuscript received May 27, 2015; revised September 18, 2015, December 3, 2015 and January 18, 2016; accepted February 10, 2016.

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This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TIE.2016.2547874, IEEE Transactions on Industrial Electronics

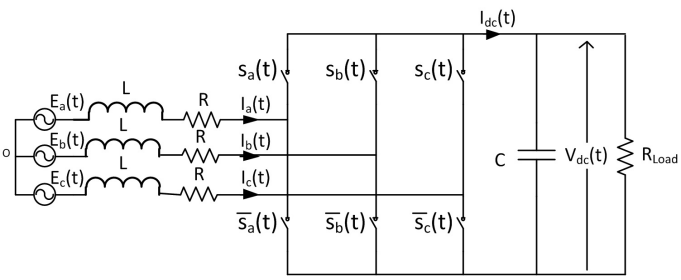

Fig. 1. Topology of a three-phase Voltage Source Rectifier

applications, again the speed outer-loop is controlled using a classic PI controller.

In this context, the objective of this paper is to show the feasibility of using cascaded MPC loops for the control of an active front-end rectifier connected to the grid and supplying a variable resistive load. The proposed MPC controllers maintain the advantages of usual MPC techniques and at the same time address the robustness issue in a computationally acceptable control algorithm. Three different cascaded MPC techniques are developed. The first one is based on controlling the inner and outer loops using two cascaded intuitive MPC strategies. These controllers calculate the input applied to the system by predicting and evaluating its future behavior. This first approach clearly shows the expected weakness of using MPC in the voltage outer-loop. The second MPC technique is based on eliminating the drawbacks of the first method while preserving its advantages. The main concept of this second MPC strategy is to eliminate unknown parameters from the dynamical model of the converter and to replace them by other quantities directly deriving from measurements. Therefore, a new dynamical model containing only measured or known variables is formulated. In the active front-end rectifier case, the load resistance value and the RL filter parameters are eliminated from the system model and replaced by the system energy consumption based on measurements. Thus, the new prediction model makes the voltage outer-loop immune to parameter variations and model inaccuracy. Moreover, the outer-loop control period choice and the energy consumption measurement technique make the robust MPC voltage outer-loop immune to measurement noises. Finally, taking advantage of the flexibility offered by the MPC paradigm, an ultimate improvement is added by imposing the use of adjacent inverter voltage vectors [16]–[18]. This results in a reduction in the switching losses of the active front-end converter.

In this paper, section II establishes the dynamical model of the active front-end rectifier connected to the grid and the resistive load. Section III develops the first cascaded MPC technique, followed in section IV by the robust dual MPC algorithm. Section V presents the switching losses reduction MPC technique. Experimental and double precision software simulation results are shown and discussed in section VI. Finally conclusions are drawn.

II. Mathematical Model of the VSR

In this section, the mathematical model of an active front-end rectifier connected to the grid and supplying a resistive load in the three-phase stationary (abc) reference frame is given (Fig. 1):

$$\frac{d\left[I_{abc}\right]}{dt} = \frac{1}{L}\left(\left[E_{abc}\right] - R\left[I_{abc}\right] - \left[u_{abc}\right]V_{dc}\right) \tag{1}$$

$$\frac{dV_{dc}}{dt} = \frac{1}{C}\left[I_a s_a + I_b s_b + I_c s_c - \frac{V_{dc}}{R_{Load}}\right] \tag{2}$$

$\left[E_{abc}\right] = \left[E_a\ E_b\ E_c\right]^T$ is the three-phase grid voltage vector and $\left[I_{abc}\right] = \left[I_a\ I_b\ I_c\right]^T$ the three-phase current vector. V_{dc} is the DC bus voltage and C the capacitor value. L and R are respectively the inductance and resistance of the RL filter and R_{Load} is the load resistance. $\left[s_{abc}\right] = \left[s_a\ s_b\ s_c\right]^T$ is the vector of the control signals of the rectifier. From this vector, one can easily derive the input voltage vector $\left[u_{abc}\right] = \left[u_a\ u_b\ u_c\right]^T$ given as:

$$\left[u_{abc}\right] = \left[s_{abc}\right] - \frac{s_a + s_b + s_c}{3}\left[1\ 1\ 1\right]^T \tag{3}$$

It is always recommended to switch to a per-unit (p.u.) model for prediction and software simulation purposes. This leads to the following p.u. model:

$$\frac{d\left[i_{abc}\right]}{dt} = \frac{1}{L}\left[Z_b\left[e_{abc}\right] - R\left[i_{abc}\right] - \left[u_{abc}\right]Z_b v_{dc}\right] \tag{4}$$

$$\frac{dv_{dc}}{dt} = \frac{1}{Z_b C}\left[i_a s_a + i_b s_b + i_c s_c\right] - \frac{v_{dc}}{C R_{Load}} \tag{5}$$

where $v_{dc} = V_{dc}/V_b$, $\left[e_{abc}\right] = \left[E_{abc}\right]/V_b$ and $\left[i_{abc}\right] = \left[I_{abc}\right]/I_b$. V_b and I_b are respectively the voltage and current base values and $Z_b = V_b/I_b$.

In order to compute the grid currents and DC bus voltage of the active front-end rectifier at a given instant, it is necessary to switch to a discrete model. The following per-unit discrete model is obtained by applying the forward Euler discretisation method to (4) and (5):

$$\left[i_{abc,k+1}\right] = c_1\left[i_{abc,k}\right] + c_2\left(\left[e_{abc,k}\right] - \left[u_{abc,k}\right]v_{dc,k}\right) \tag{6}$$

$$v_{dc,k+1} = c_3 V_{dc,k} + c_4\left[s_{a,k} i_{a,k} + s_{b,k} i_{b,k} + s_{c,k} i_{c,k}\right] \tag{7}$$

where $c_1 = 1 - T\frac{R}{L}$, $c_2 = Z_b\frac{T}{L}$, $c_3 = 1 - \frac{T}{C R_{Load}}$ and $c_4 = \frac{T}{Z_b C}$. T is the calculation step period. $\left[i_{abc,k}\right]$, $\left[e_{abc,k}\right]$, $\left[s_{abc,k}\right]$ and $v_{dc,k}$ are respectively the p.u. source currents, grid voltages, switches states and capacitor voltage at kT.

Equations (6) and (7) are used for simulation purposes and to predict the active front-end rectifier grid currents and DC voltage for control purposes. In the prediction case, the calculation step period T is equal to the sampling period T_s.

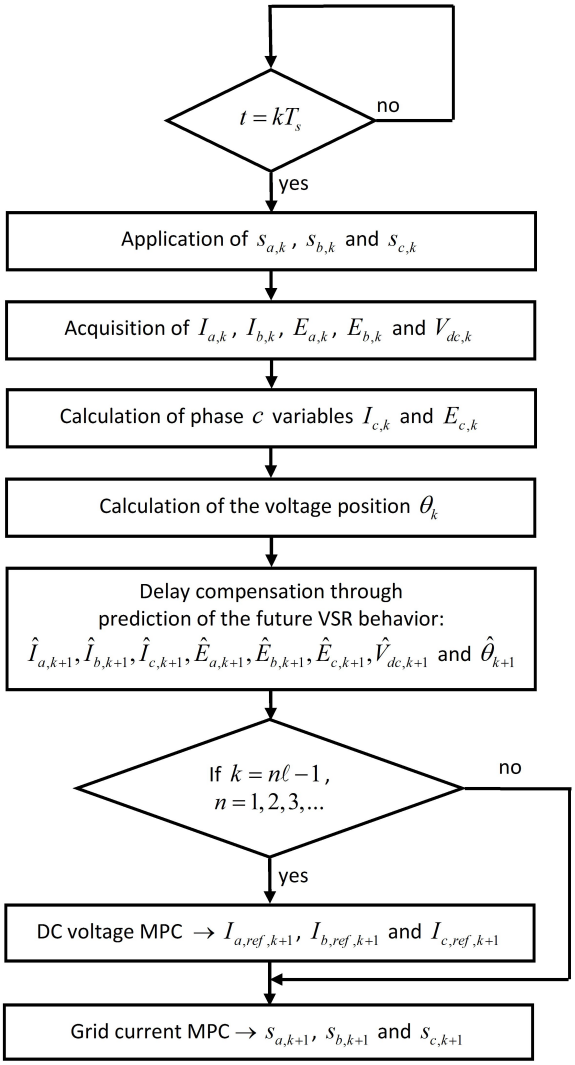

Fig. 2. Cascaded dual-MPC algorithm

III. Cascaded Dual MPC

This section develops a first, intuitive cascaded dual MPC technique, for the control of an active front-end rectifier connected to the grid supplying a variable resistive load. The two cascaded MPC controllers use the dynamical model of the system in order to predict its future behavior [19], [20]. The prediction results are evaluated and the switches states which minimize a defined cost function are applied to the system.

The control algorithm objectives are:

- To reach and maintain V_{dc} at its reference value $V_{dc,ref}$
- To obtain a unit power factor on the grid side.

The proposed cascaded dual MPC algorithm (Fig. 2) is applied at each kT_s and starts with the application of the previously computed switches states $s_{a,k}$, $s_{b,k}$ and $s_{c,k}$ and the acquisition of the active front-end rectifier variables $I_{a,k}$, $I_{b,k}$, $E_{a,k}$, $E_{b,k}$ and $V_{dc,k}$. Phase c variables are then computed as $I_{c,k} = -I_{a,k} - I_{b,k}$ and $E_{c,k} = -E_{a,k} - E_{b,k}$. $E_{a,k}$, $E_{b,k}$ and $E_{c,k}$ are used to compute the angular position θ_k of the grid voltage vector using a Dual Second Order Generalized Integrator (DSOGI) Phase Locked Loop (PLL) [21]. The PLL is followed by a delay compensation method that eliminates the delay introduced by the control law. At this stage the two MPC algorithms are applied. The outer-loop DC voltage MPC has a control period of ℓT_s where ℓ is an integer > 1. This means that the outer-loop is calculated at instant $k = n\ell - 1$ where $n = 1, 2, 3, ...$. Thus, the DC voltage loop refreshes the current references $I_{a,ref,k+1}$, $I_{b,ref,k+1}$ and $I_{c,ref,k+1}$ that the system has to track in order for the capacitor voltage to reach the value $V_{dc,ref}$ in a time interval of ℓT_s. Then, having the grid current references, the inner-loop grid current MPC generates every T_s the control signals $s_{a,k+1}$, $s_{b,k+1}$ and $s_{c,k+1}$ to be applied to the rectifier in order to track these current references.

A. Delay compensation [20]

In a real-time implementation, the time required to compute the control algorithm takes a significant portion of the sampling period, resulting in one sampling period delay. The effect of this delay has an impact on the controller performance, therefore a delay compensation scheme must be implemented.

Knowing the system dynamical model, the variables $I_{a,k}$, $I_{b,k}$, $E_{a,k}$, $E_{b,k}$, θ_k and $V_{dc,k}$ and the inputs $s_{a,k}$, $s_{b,k}$ and $s_{c,k}$ being applied at kT_s, new variables are predicted for instant $(k+1)T_s$: $\hat{I}_{a,k+1}$, $\hat{I}_{b,k+1}$, $\hat{E}_{a,k+1}$, $\hat{E}_{b,k+1}$, $\hat{\theta}_{k+1}$ and $\hat{V}_{dc,k+1}$. $\hat{I}_{c,k+1}$, $\hat{E}_{c,k+1}$ are deduced as previously mentioned. Those predictions are then used as initial conditions for both MPC controllers in the voltage and grid current loops.

B. Outer-Loop DC Voltage MPC

The outer-loop DC voltage MPC consists in an optimization problem that is solved online and that can be summarized as follows:

$$J_{outer} = \mid V_{dc,k+\ell} - V_{dc,ref} \mid \tag{8}$$

Subject to the following constraints:

$$\begin{aligned} I_{ref,k+1} &< I_{max} \\ I_{ref,k+1} &> -I_{max} \end{aligned} \tag{9}$$

where $I_{ref,k+1}$ is the three-phase RMS reference current that the MPC must generate in order for the capacitor voltage to reach $V_{dc,ref}$ in a time interval of ℓT_s, starting from $(k+1)\,T_s$, and where $\sqrt{2}I_{max}$ is the maximum admissible current value.

This optimization problem uses a prediction horizon equal to one. It is subject to linear constraints that limits the reference grid currents within the interval $[-I_{max}, I_{max}]$. $V_{dc} = f(I_{ref})$ is a continuous increasing function, thus the solution of the optimization problem can be computed by applying the following steps:

- Calculate $I_{ref,k+1}$ that leads to $V_{dc,k+\ell} = V_{dc,ref}$.
- Saturate $I_{ref,k+1}$ within the interval $[-I_{max}, I_{max}]$.

To formulate the outer-loop DC voltage control law, the following assumptions are considered:

- The grid currents are correctly tracking their references.
- The losses inside the converter are ignored.
- The grid voltages are balanced.

- The energy variation inside the RL filter inductor is ignored.

The power transiting from the grid to the load side is constant and equal to:

$$P = 3EI_{ref,k+1} \tag{10}$$

where E is the RMS grid voltage value. When applying a constant power to the load side of the VSR (capacitor parallel to R_{Load}), the capacitor voltage variation can be written as:

$$P = \frac{V_{dc}^2}{R_{Load}} + CV_{dc}\frac{dV_{dc}}{dt} \tag{11}$$

The solution of (11) gives the evolution of the capacitor voltage over the time:

$$V_{dc}(t) = \sqrt{V_{dc}^2(0)e^{\frac{-2t}{CR_{Load}}} + \left(1 - e^{\frac{-2t}{CR_{Load}}}\right)PR_{Load}} \tag{12}$$

where $V_{dc}(0)$ is the initial condition of the capacitor voltage.

In order for the capacitor voltage to reach $V_{dc,ref}$ in time interval ℓT_s, and starting from $V_{dc}(0) = \hat{V}_{dc,k+1}$, the power that must be given to the load side can be calculated as:

$$P = \frac{V_{dc,ref,k}^2 - \hat{V}_{dc,k+1}^2 e^{\frac{-2\ell T_s}{CR_{Load}}}}{R_{Load}\left(1 - e^{\frac{-2\ell T_s}{CR_{Load}}}\right)} \tag{13}$$

The current reference magnitude can then be deduced using (10) and (13):

$$I_{ref,k+1} = \frac{\left[V_{dc,ref,k}^2 - \hat{V}_{dc,k+1}^2 e^{\frac{-2\ell T_s}{CR_{Load}}}\right]}{3ER_{Load}\left(1 - e^{\frac{-2\ell T_s}{CR_{Load}}}\right)} \tag{14}$$

This current reference is finally limited to the interval $[-I_{max}, I_{max}]$.

Knowing the grid voltage vector position $\hat{\theta}_{k+1}$ at time $(k+1)\,T_s$, the three-phase current references are then computed using a sine function generator as follows:

$$[I_{abc,ref,k+1}] = \sqrt{2}I_{ref,k+1}cos\left(\theta_{k+1} - [\varphi]\right) \tag{15}$$

with $[I_{abc,ref,k+1}] = [I_{a,ref,k+1}\ I_{b,ref,k+1}\ I_{c,ref,k+1}]^T$ and $[\varphi] = \left[0\ \frac{2\pi}{3}\ \frac{4\pi}{3}\right]^T$.

C. Inner-Loop Grid Currents MPC

The inner-loop grid currents MPC generates every T_s the inputs $s_{a,k+1}$, $s_{b,k+1}$ and $s_{c,k+1}$ to be applied to the VSR rectifier at instant $(k+1)T_s$ in order to track the current references refreshed with period ℓT_s. The algorithm starts by predicting the grid currents at instant $(k+2)T_s$ for all possible configurations of the power switches. It uses the predicted output variables of the delay compensation method. Since there are three input variables s_a, s_b and s_c, it is possible to generate eight configurations of the power switches, seven leading to different results. The computation of the discrete dynamical model results in seven different sets of predicted grid currents $S_i = \left\{\hat{I}_{a,k+2,i}, \hat{I}_{b,k+2,i}, \hat{I}_{c,k+2,i}\right\}$ with $i = 0, \cdots, 6$. Each set S_i is evaluated using the cost function given in (16). The configuration of the power switches that leads to the minimization of the cost function J is applied to the system at instant $(k+1)T_s$ [22].

$$\begin{aligned} J = &\left|I_{a,ref,k+2} - \hat{I}_{a,k+2}\right| + \left|I_{b,ref,k+2} - \hat{I}_{b,k+2}\right| \\ &+ \left|I_{c,ref,k+2} - \hat{I}_{c,k+2}\right| \end{aligned} \tag{16}$$

D. Robustness of Cascaded Dual-MPC

The current inner-loop implies the use of (6) which integrates the resistance and the inductance value of the RL filter. Since, the RL filter parameters are known and not subject to major variations, the prediction results are accurate. Therefore, the robustness problem is not a major issue in the inner-loop design.

However, the voltage outer-loop has to track the capacitor voltage reference value and to compensate current tracking errors. Therefore, it must be robust against parametric variations. The proposed outer-loop is based on the calculation of (14) which is a function of the RMS grid voltage E, the capacitor C and the load resistance R_{Load}. E is detected by the PLL. The capacitor voltage value C is a known parameter related to the converter structure and not subject to major variations. But the load resistance R_{Load} is a variable parameter affecting the prediction process. Consequently, the capacitor voltage reference is not correctly tracked and presents some bias in case of load variations as shown in the results section.

IV. Robust Cascaded Dual-MPC

The previous section proposed a cascaded dual-MPC which shows the weakness of using MPC techniques in outer-loops. This issue can be resolved by using a new robust cascaded dual-MPC based on an original outer-loop DC voltage MPC algorithm.

This algorithm solves the same optimization problem as in section III.B and has the same structure as the one presented in Fig. 2 but two main differences exist:

- The calculation of the energy supplied by the grid.
- A new outer-loop robust MPC method.

Thus, after measuring and calculating the grid currents and voltages at kT_s, the variation of energy $e_{G,k}$ supplied by the grid between kT_s and $(k+1)\,T_s$ is calculated as follows:

$$e_{G,k} = \left[E_{a,k}I_{a,k} + E_{b,k}I_{b,k} + E_{c,k}I_{c,k}\right]T_s \tag{17}$$

The total energy supplied by the grid is then given by:

$$E_{G,k+1} = E_{G,k} + e_{G,k} \tag{18}$$

The angular position θ_k is then calculated using a DSOGI PLL and the delay compensation method is applied followed by the inner-loop grid currents MPC algorithm.

The new robust outer-loop DC voltage MPC is based on a new formulation of the dynamical model of the system. This

model links the capacitor voltage value to the energy supplied by the grid and eliminates the use of the variable parameter R_{Load} from the system dynamical equations. It also eliminates the RL filter parameters from the system equations. The use of only measurable quantities allows the proposed MPC to be more robust against the parametric variations and mitigates model imperfections. Moreover, by varying the parameter ℓ it is possible to increase or decrease the MPC outer-loop sensibility to measurement noise. Thus, by increasing the parameter ℓ the outer-loop algorithm reacts slowly to any variation of the load or of the DC link voltage but it will be less sensitive to measurement noise on the other hand by decreasing ℓ the system reacts quickly but it will be more sensitive to measurement noise. This property is also valid for the first outer-loop DC voltage MPC developed in section III.B. In the following, the assumptions presented at the beginning of section III.B are maintained.

The energy transiting from the grid to the load side between kT_s and $(k+\ell)\,T_s$ is given in (19) and is supposed to be fully transferred to the load side.

$$E_{T,k} = 3EI_{ref,k+1}\ell T_s \tag{19}$$

Viewed from the load side, $E_{T,k}$ is the energy that must be stored in the capacitor and given to the load resistance in order for the capacitor voltage to reach $V_{dc,ref,k}$ at the end of the next time interval of length ℓT_s. Thus $E_{T,k}$ is divided into two parts:

- $E_{C,k}$ is the energy needed in order for the capacitor voltage to reach its reference value $V_{dc,ref,k}$.
- $E_{R,k}$ is the energy consumed by the load resistance during the next time interval of length ℓT_s.

Thus, $E_{T,k}$ can be written as follows:

$$E_{T,k} = \underbrace{\frac{1}{2}C\left(V_{dc,ref,k+1}^2 - \hat{V}_{dc,k+1}^2\right)}_{E_{C,k}} + E_{R,k} \tag{20}$$

The energy $E_{R,k}$ is not known and needs to be calculated. Therefore, considering that the energy E_R varies slowly over time, it is possible to assume that $E_{R,k} = E_{R,k-\ell}$ where $E_{R,k-\ell}$ is calculated at instant kT_s using measurable values as follows:

$$E_{R,k} = E_{R,k-\ell} = \Delta E_{G,k} - \frac{1}{2}C\left(V_{dc,k}^2 - V_{dc,k-\ell}^2\right) \tag{21}$$

$\Delta E_{G,k} = E_{G,k} - E_{G,k-\ell}$ is the energy supplied by the grid between kT_s and $(k-\ell)\,T_s$. It should be mentioned that the value of $V_{dc,k-\ell}$ and $E_{G,k-\ell}$ are measured and stored.

Finally, using (19), (20) and (21) the current reference is calculated as:

$$I_{ref,k+1} = \frac{\frac{1}{2}C\left(V_{dc,ref,k+1}^2 - \hat{V}_{dc,k+1}^2\right) + E_{R,k}}{3E\ell T_s} \tag{22}$$

This method is immune to load parametric variations and to measurement noise, thus eliminating the weakness of the first proposed dual MPC controller.

TABLE I
COMPLEMENTARY ACTIVE FRONT-END RECTIFIER CONFIGURATIONS

Configurations	**1**	**2**	**3**	**4**
$s_{a,k+1}$	$s_{a,k}$	$s_{a,k}$	$s_{a,k}$	$not\,(s_{a,k})$
$s_{b,k+1}$	$s_{b,k}$	$s_{b,k}$	$not\,(s_{b,k})$	$s_{b,k}$
$s_{c,k+1}$	$s_{c,k}$	$not\,(s_{c,k})$	$s_{c,k}$	$s_{c,k}$

V. ROBUST CASCADED MPC ALGORITHM WITH REDUCED SWITCHING LOSSES

This section develops a cascaded dual-MPC algorithm that reduces the switching losses inside the active front-end rectifier. MPC controllers having the benefit of being flexible and easy to tune, a further improvement can be achieved to the previous algorithm, presented in section IV, by modifying the current inner-loop of section III.C.

Knowing the predicted three-phase grid currents $\hat{I}_{a,k+1}$, $\hat{I}_{b,k+1}$, $\hat{I}_{c,k+1}$, the reference currents $\hat{I}_{a,ref,k+1}$, $\hat{I}_{b,ref,k+1}$, $\hat{I}_{c,ref,k+1}$ and voltages $\hat{E}_{a,k+1}$, $\hat{E}_{b,k+1}$, $\hat{E}_{c,k+1}$, along with the active front-end rectifier dynamical model, it is possible to predict the future behavior of the system for all possible feasible configurations of the power switches. Moreover, knowing that the input variables s_a, s_b and s_c are binary values, it is possible to generate up to eight configurations of the voltage vector, seven of them leading to different values. The objective of this MPC inner-loop is to reduce the number of commutations per sampling period. Instead of allowing all the possible configurations, this approach uses a restrained number of configurations shown in Table I. The four chosen configurations imply that two or less switches are commutating at each sampling period, whereas the three eliminated configurations have either four or six switches commutating at the same time. Applying a Concordia or Clark transform helps to deduce that the four selected configuration are consecutive to the previously calculated input $s_{a,k}$, $s_{b,k}$, $s_{c,k}$ in the α,β frame. A similar approach had been proposed in [16]–[18]. In our case this control strategy is not an original contribution, nevertheless this strategy shows the flexibility of the MPC approaches, and also improves the current inner-loop of the system.

In the rest of this paper mpc_1 stands for the cascaded dual-MPC controller presented in section III. mpc_2 is the robust dual MPC controller of section IV and mpc_3 in the robust reduced losses controller presented in this section.

Since the number of allowed switch configurations is limited to four, this inner-loop MPC algorithm needs less calculation effort than the inner-loop of mpc_1 and mpc_2.

The chosen configurations along with the discrete dynamical model of the system allow the calculation of a new set of grid currents $S_i = \left\{\hat{i}_{a,k+2,i}, \hat{i}_{b,k+2,i}, \hat{i}_{c,k+2,i}\right\}$ with $i = 0, \cdots, 3$. Each set S_i is evaluated using the cost function in (16). The configuration of the power switches that leads to the minimization of the cost function J is applied to the system at instant $(k+1)\,T_s$.

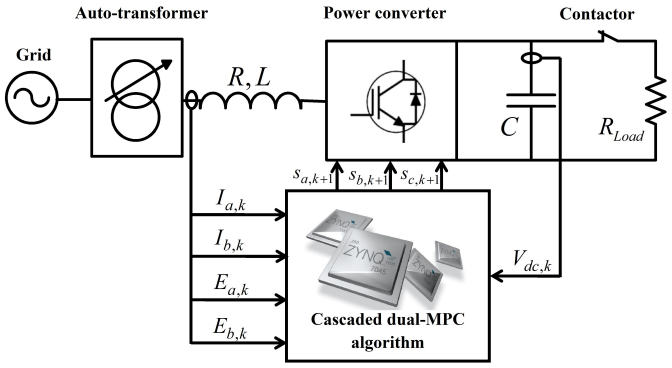

Fig. 3. Testbench structure

TABLE II
POWER SYSTEM PARAMETERS

Description	Parameters	Values	Units
RL filter inductance	L	20	mH
RL filter resistance	R	0.8	Ω
Load resistance	R_{Load}	200	Ω
Capacitance	C	1100	μF
Three phase grid amplitude	$E\sqrt{2}$	110	V
Three phase grid frequency	f_E	50	Hz
Sampling period	T_s	50	μs

TABLE III
ALGORITHMS COMPUTATION TIME

Algorithms	$mpc1$	$mpc2$	$mpc3$
Duration	$17.5\mu s$	$20\mu s$	$18.2\mu s$

VI. SOFTWARE SIMULATION AND EXPERIMENTAL RESULTS

This section presents double precision software simulation results as well as experimental results of the three dual cascade MPC techniques previously developed. The simulation model consists on solving the active front-end rectifier equations presented in section II at high frequencies in order to achieve a quasi-continuous simulation, then the Dual MPC algorithm is implemented as in Fig. 2. The whole simulation model was coded using C/C++ language and the results were exploited using MATLAB graphic tools. In this section the test bench is first introduced along with the control specifications of the system. Evaluation criteria are then defined. Software simulation and experimental results are presented to validate the feasibility of the proposed algorithms. The results of the ideal conditions are firstly presented, followed by the robustness tests then the evaluation of the number of commutations for each MPC strategy. Finally, in order to focus on the benefits of using MPC controllers in outer-loops, a comparison between MPC and classic PI controllers for outer-loop control purposes is developed.

A. Testbench presentation and control specifications

The testbench shown in Fig. 3 consists of the grid three-phase voltage source $230V$, $50Hz$ connected to an auto-transformer providing a voltage RMS output equal to E. It is connected to a three-phase RL filter then to a $20KVA$ three-phase Semikron power converter (PWM rectifier) composed of IGBT/Diode switches. On the load side of the converter, the components are the DC-link capacitor $(1100\mu F/800V)$, a load resistance supporting a maximum current of $2.5A$ and a contactor used to connect and disconnect the load resistance. The power system parameters are presented in Table II.

Each switch of the VSR rectifier includes an IGBT with an anti-parallel diode. Initially all IGBTs are OFF but the diodes are functional. So the six switch power converter is equivalent to a six diodes rectifier and the capacitor voltage initial value is equal to $180V$.

The control algorithms are implemented on a Zedboard Zynq-7000 All Programmable (AP) System on-Chip (SoC). This digital device is an FPGA-based SoC platform recently introduced by Xilinx. It integrates an FPGA fabric, a dual-core ARM Cortex-A9 processor running at 667 MHz and two 12 bits, 1 Mega Sample Per Second (MSPS) Analog to Digital Converters (ADCs).

The control algorithms and the DSOGI PLL are implemented in the Zynq-7000 processing part while the FPGA fabric part is responsable for applying the calculated switches states to the active front-end rectifier. The maximum time needed by a control algorithm consists of: the ADC conversion time and the DSOGI PLL, the inner and outer-loop computation time. The time needed by each control method is presented in table III. The results show that the algorithm computation time is always less than the sampling period and that mpc_3 inner-loop needs less computational effort than mpc_2 and thus than mpc_1.

The control parameters are given in the following:

- The capacitor DC voltage reference $V_{dc,ref}$ is equal to 300V.
- The grid maximum current $\sqrt{2}I_{max}$ is equal to 4A.
- The inner-loop is computed $\ell = 200$ times faster than the outer-loop.

B. Evaluation criteria

In order to compare the three proposed MPC techniques, three evaluation criteria are defined. The first evaluation criterion ϵ_1 is the sum of the absolute value of the capacitor voltage error and it is given by:

$$\epsilon_{1,k} = \sum_{i=0}^{k} |V_{dc,ref,i} - V_{dc,i}| \tag{23}$$

The second and third evaluation criteria ϵ_2 and ϵ_3 are the discrete integrals of the absolute value of the grid reactive and active powers. They highlight the power factor tracking errors and are given by:

$$\epsilon_{2,k} = \sum_{i=0}^{k} |Q_i| \, T_s \tag{24}$$

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$$\epsilon_{3,k} = \sum_{i=0}^{k} |P_i| \, T_s \tag{25}$$

where Q is the instantaneous reactive power and P the instantaneous active power.

$$Q = \frac{-\left[(E_a - E_b)I_c + (E_b - E_c)I_a + (E_c - E_a)I_b\right]}{\sqrt{3}} \tag{26}$$

$$P = E_a I_a + E_b I_b + E_c I_c \tag{27}$$

C. Simulation and experimental results in ideal conditions

In this section, the simulation and experimental results are performed in the case where the parameters of the system are known and constant. Double precision software simulation results are shown in Fig. 4, 5 and 6 for the three proposed methods. Fig. 4 shows the capacitor voltage, Fig. 5 the phase a voltage, currents and current references and Fig. 6 presents the calculated evaluation criteria.

The results show that the three cascaded dual-MPC controllers lead to the same performances. The control objectives are respected. Indeed, the capacitor voltage and the grid currents are correctly tracking their references. Furthermore, Fig. 5 shows that there is no phase shift between phase a voltage and current. Moreover, Fig. 6 shows that ϵ_2 is very close to 0 and $\epsilon_2 << \epsilon_3$. Finally, a unit power factor is achieved.

In the same ideal conditions, an experimental test is performed and results are shown in Fig. 7, 8 and 9. The evaluation criteria show that the three MPC controllers mpc_1, mpc_2 and mpc_3 lead to the same performances. The THD of phase a current at steady state is approximately the same for the three control methods and it is equal to 6.7%, 7.2% and 7.3% for mpc_1, mpc_2 and mpc_3 respectively. The small difference between mpc_1 and mpc_2 or mpc_3 is due to the voltage outer-loop strategy. Indeed, mpc_2 and mpc_3 use an adaptive prediction model based on measurements. This model is thus an approximation of the exact model used in mpc_1. Therefore, when the parameters are perfectly known in the ideal case, mpc_1 shows the best results in terms of THD. The control objectives are respected, and the experimental results validate the previous double precision simulation results.

The simulation and experimental results presented in the case of ideal conditions validate the feasibility of the three proposed algorithms. The weaknesses of the first algorithm are however still hidden and will be shown in the following section.

D. Experimental robustness tests

Assuming that the load resistance value is unknown and is estimated equal to 300Ω instead of 200Ω, the previously described experimental test is repeated and experimental results are shown in Fig. 10 and 11.

The evaluation criteria ϵ_1 is diverging for mpc_1 and shows that this first algorithm does not track the capacitor voltage

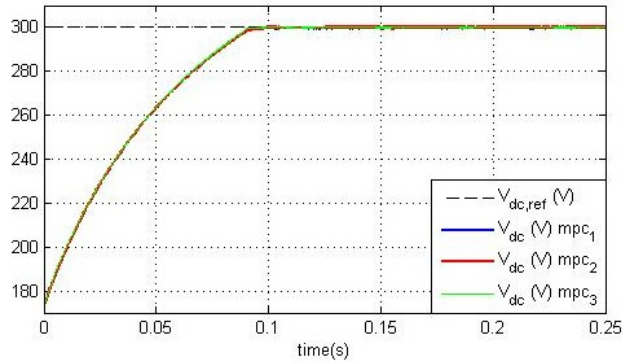

Fig. 4. Capacitor voltage simulation results

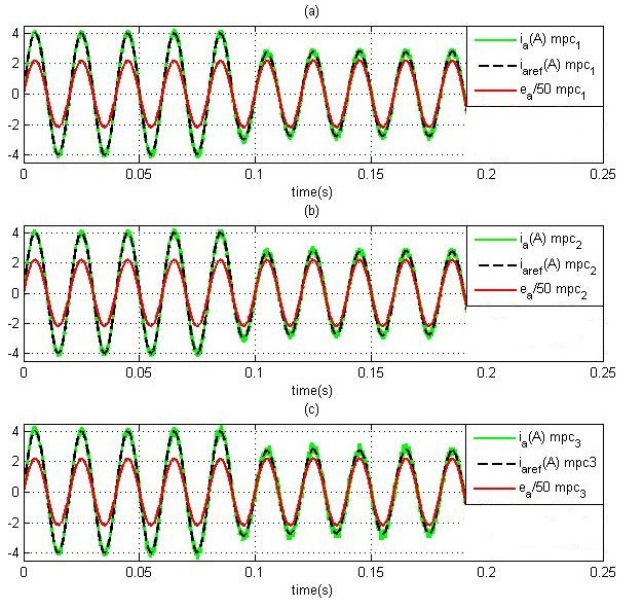

Fig. 5. Phase a voltage and current simulation results for (a) mpc_1, (b) mpc_2 and (c) mpc_3

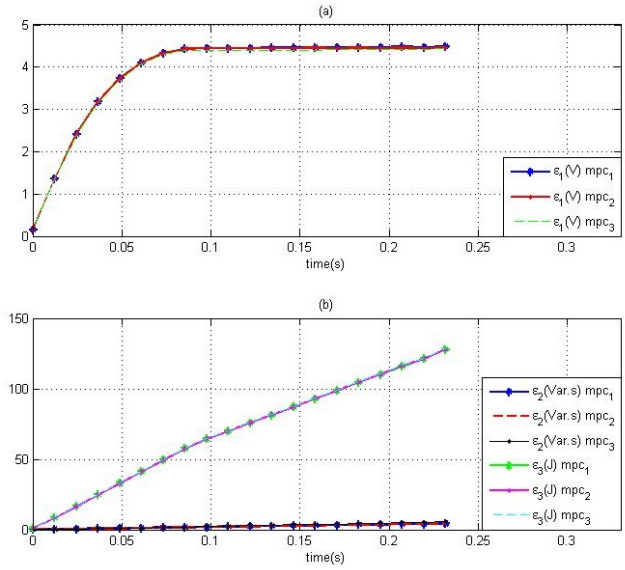

Fig. 6. Simulation results (a) ϵ_1 evaluation criterion (b) ϵ_2 and ϵ_3 evaluation criteria

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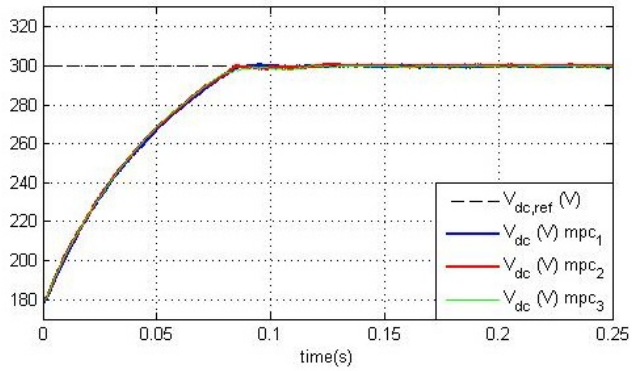

Fig. 7. Capacitor voltage experimental results

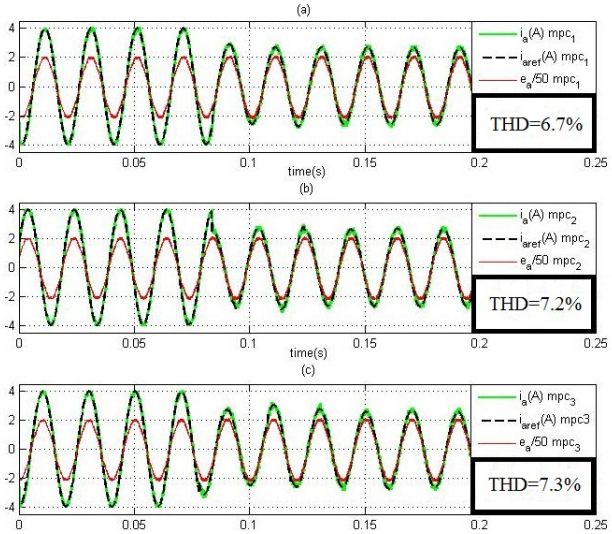

Fig. 8. Phase a voltage and current experimental results for (a) mpc_1, (b) mpc_2 and (c) mpc_3

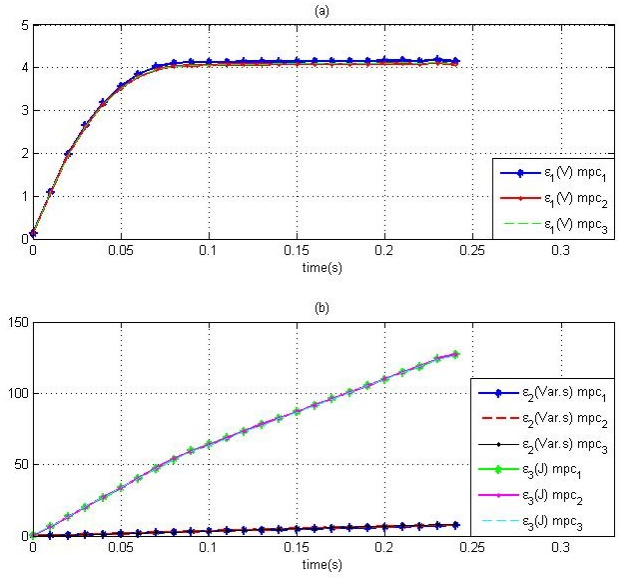

Fig. 9. Experimental results (a) ϵ_1 evaluation criterion (b) ϵ_2 and ϵ_3 evaluation criteria

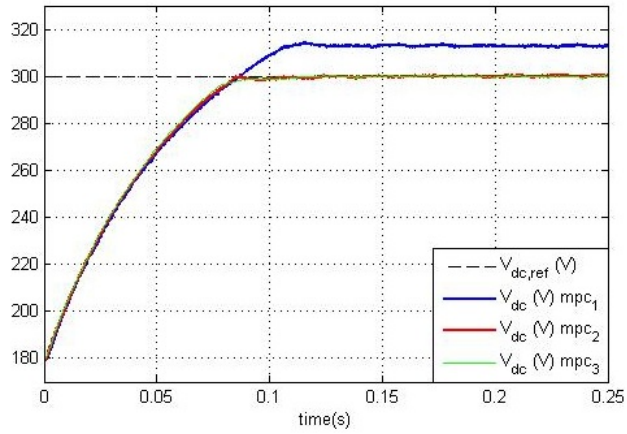

Fig. 10. Robustness test: capacitor voltage experimental results

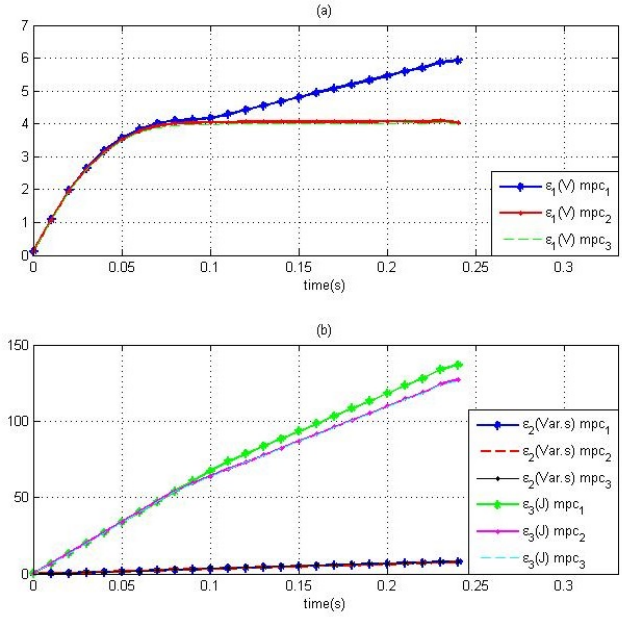

Fig. 11. Robustness test: experimental results (a) ϵ_1 evaluation criterion (b) ϵ_2 and ϵ_3 evaluation criteria

reference. This test shows the weaknesses of using standard MPC controller in the outer-loops. The proposed robust MPC controllers mpc_2 and mpc_3 are however able to track the DC voltage reference, thus validating their immunity against parametric variations. It should be mentioned that a unit power factor is achieved for all methods.

In order to confirm the robustness of mpc_2, another test is performed. It consists on disconnecting then reconnecting the load resistance $R_{Load} = 200\Omega$. The capacitor voltage and the grid currents are shown in Fig. 12 and 13. This test shows that even in worst case scenario, the proposed control law stays robust and tracks the references.

E. Energy losses in the converter

The switching losses in the converter are linked to the number of commutations of each power switch. Therefore, in order to evaluate the switching losses associated to each

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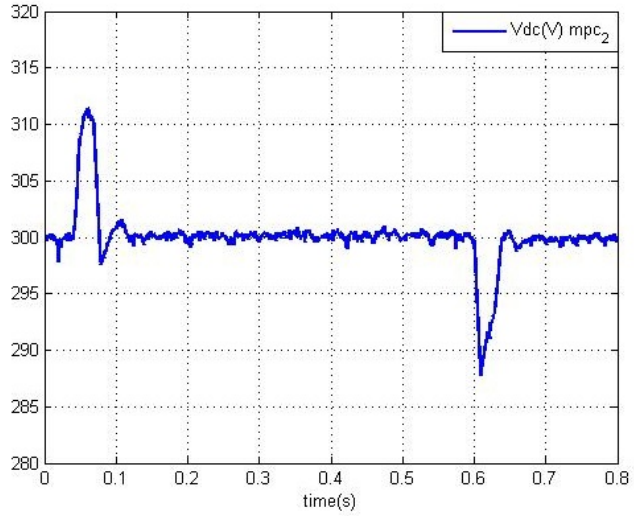

Fig. 12. Capacitor voltage experimental results to the disconnection than connection of the resistance load

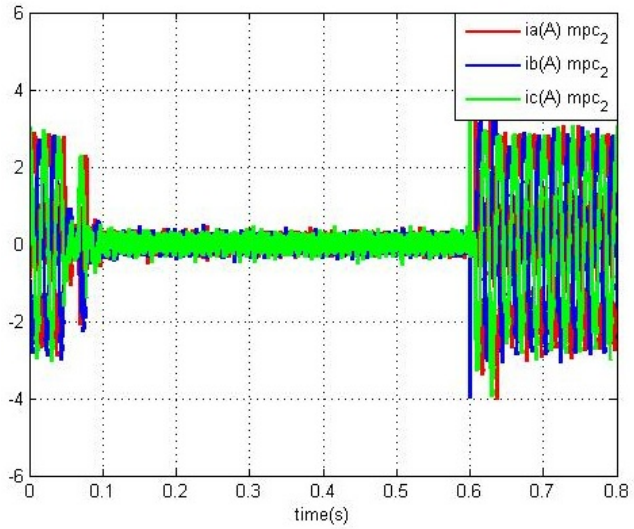

Fig. 13. Grid currents experimental results to the disconnection than connection of the resistance load

TABLE IV
AVERAGE SWITCHING FREQUENCY AT STEADY STATE

Methods	mpc_1	mpc_2	mpc_3
Average switching frequency	$4500Hz$	$4500Hz$	$3200Hz$

control strategy, the average switching frequency at steady state is presented in table IV. This table shows that mpc_3 induces less switching losses since the switches commutate approximately one third $(1/3)$ less times than in mpc_1 and mpc_2.

F. Benefits of using MPC in outer-loops

In this section the simulation results of mpc_3 are compared to the results of an MPC scheme where the outer-loop is a PI-based controller and the inner-loop is the MPC-based controller presented in Section V. The PI controller is calculated as follows:

- In order to make the control problem linear and thus more compatible with a PI regulation, the square of the capacitor voltage V_{dc}^2 is controlled.
- A saturation block is used in order to limit the current within the interval $[-I_{max}, I_{max}]$.
- An anti-wind-up gain is used to eliminate the integral saturation effect.
- The gains of the PI controller are calculated to approach as closely as possible the performances obtained with MPC controllers.

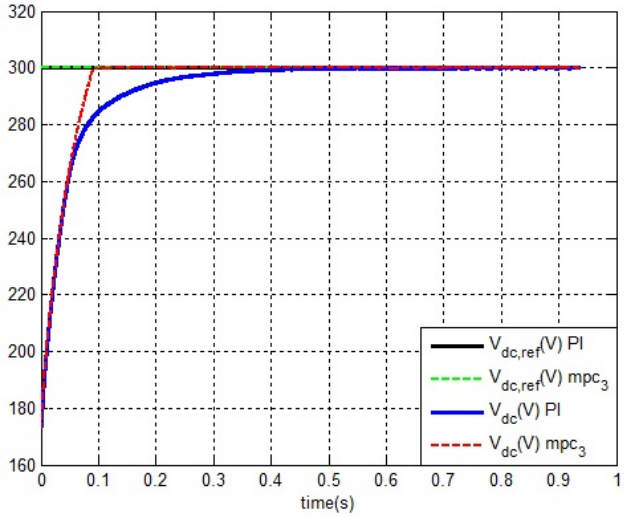

Fig. 14. Capacitor DC voltage simulation results for mpc_3 and an outer-loop PI controller

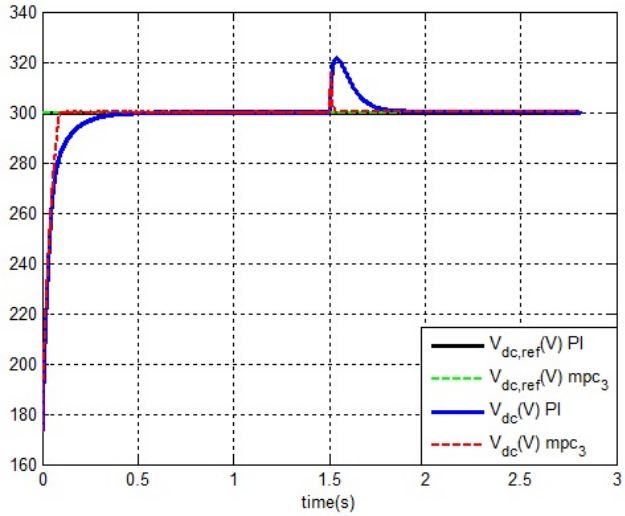

Fig. 15. Capacitor DC link voltage robustness test for mpc_3 and an outer-loop PI controller

Fig. 14 shows that when the capacitor voltage is close to its reference value, the PI controller slows the dynamic of the response, this leads to mpc_3 having a better time response than the PI. A robustness test is then presented in Fig. 15 where the load resistance R_{Load} is disconnected at instant

$t = 1.5s$. The simulation results show that both controllers track the reference voltage at steady state but mpc_3 has a smaller overshoot and is responding faster. In conclusion, the proposed mpc_3 maintains the benefits of MPC controller while dealing with their drawbacks, mainly the robustness issue.

VII. Conclusions

This paper presents three different cascaded dual-MPC techniques for the control of an active front-end rectifier connected to the grid and supplying a variable resistive load. The first controller uses standard MPC algorithm based on predicting the future behavior of the system then evaluating the predicted results. The experimental results show that this first method introduces a bias in the capacitor voltage value resulting from a bad estimation of the load resistance value. A new robust dual MPC cascaded algorithm is then introduced. This algorithm is based on the formulation of a new prediction model of the system where the system variable parameters are replaced with new formulated parameters based on measurements. In the active front-end rectifier case the resistive load value and the RL filter parameters are eliminated from the system prediction model. Instead, the new model includes the estimated energy consumed by the load. Experimental results validate the proposed algorithm. Finally, taking advantage of the flexibility of MPC controllers, a method reducing the switching losses is also presented and experimentally validated. Perspectives to this work is to examine and improve the performance of the proposed control strategies under distorted and unbalanced grid voltage.

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